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**Heterogeneous Reconfigurable Processors for Real-Time Baseband Processing**-Chenxin Zhang 2016-01-18
This book focuses on domain-specific heterogeneous reconfigurable architectures, demonstrating for readers a computing platform which is flexible enough to support multiple standards, multiple modes, and multiple algorithms. The content is multi-disciplinary, covering areas of wireless communication, computing architecture, and circuit design. The platform described provides real-time processing capability with reasonable implementation cost, achieving balanced trade-offs among flexibility, performance, and hardware costs. The authors discuss efficient design methods for wireless communication processing platforms, from both an algorithm and architecture design perspective. Coverage also includes computing platforms for different wireless technologies and standards, including MIMO, OFDM, Massive MIMO, DVB, WLAN, LTE/LTE-A, and 5G.

**Dynamic System Reconfiguration in Heterogeneous Platforms**-Nikolaos Voros 2009-05-28 Dynamic System Reconfiguration in Heterogeneous Platforms defines the MORPHEUS platform that can join the performance density advantage of reconfigurable technologies and the easy control capabilities of general purpose processors.

It consists of a System-on-Chip made of a scalable system infrastructure hosting heterogeneous reconfigurable accelerators, providing dynamic reconfiguration capabilities and data-stream management capabilities.

**A Design Methodology for Low-power Heterogeneous Reconfigurable Digital Signal Processors**-Marlene Wan 2001

**Proceedings of the 5th International Workshop on Reconfigurable Communication-centric Systems on Chip 2010 - ReCoSoC**-Michael Hübler 2010

**Low-power Heterogeneous Reconfigurable Digital Signal Processors with Energy-efficient Interconnect Network**-Hui Zhang (Ph.D.) 2004

**Reconfigurable Computing**-Joao Cardoso 2011-08-17 As the complexity of modern embedded systems increases, it becomes less practical to design monolithic processing platforms. As a result, reconfigurable computing is being adopted widely for more flexible design. Reconfigurable Computers offer the spatial parallelism and fine-grained customizability of application-specific circuits with the postfabrication programmability of software. To make the most of this unique combination of performance and flexibility, designers need to be aware of both hardware and software issues. FPGA users must think not only about the gates needed to perform a computation but also about the software flow that supports the design process. The goal of this book is to help designers become comfortable with these issues, and thus be able to exploit the vast opportunities possible with reconfigurable logic.

**Massive MIMO Detection Algorithm and VLSI Architecture**-Leibo Liu 2019-02-20 This book introduces readers to a reconfigurable chip architecture for future wireless communication systems, such as 5G and beyond. The proposed architecture perfectly meets the demands for future mobile communication solutions to support different standards, algorithms, and antenna sizes, and to accommodate the evolution of standards and algorithms. It employs massive MIMO detection algorithms, which combine the advantages of low complexity and high parallelism, and can fully meet the requirements for detection accuracy. Further, the architecture is implemented using ASIC, which offers high energy efficiency, high area efficiency and low detection error. After introducing massive MIMO detection algorithms and circuit architectures, the book describes the ASIC implementation for verifying the massive MIMO detection. In turn, it provides detailed information on the proposed reconfigurable architecture: the data path and configuration path for massive MIMO detection algorithms, including the processing unit, interconnections, storage mechanism, configuration information format, and configuration method.

**The Application of Programmable DSPs in Mobile Communications**-Alan Gatherer 2001-12-21 With the introduction of WAP in Europe and I-mode in Japan, mobile terminals took their first steps out of the world of mobile telephony and into the world of mobile data. At the same time, the shift from 2nd generation to 3rd generation cellular technology has increased the potential data rate available to mobile users by tenfold as well as shifting data transport from circuit switched to packet data. These fundamental shifts in nature and the quantity of data available to mobile users has led to an explosion in the number of applications being developed for future digital terminal devices. Though these applications are diverse they share a common need for complex Digital Signal Processing (DSP) and in most cases benefit from the use of programmable DSPs (Digital Signal Processors). * Features contributions from experts who discuss the implementation and applications of programmable DSPs * Includes detailed introductions to speech coding, speech recognition, video and audio compression, biometric identification and their application for mobile communications devices * Discusses the alternative DSP technology which is attempting to unseat the programmable DSP from the heart of tomorrow’s mobile terminals * Presents innovative new applications that are waiting to be discovered in the unique environment created when mobility meets signal processing * The Application of Programmable DSPs in Mobile Communications provides an excellent overview for engineers moving into the area of mobile communications or entrepreneurs looking to understand state of the art in mobile terminals. It is also a must for students and professors looking for new application areas where DSP technology is being applied.

New Algorithms, Architectures and Applications for Reconfigurable Computing
Patrick Lysaght
2005-12-05 New Algorithms, Architectures and Applications for Reconfigurable Computing consists of a collection of contributions from the authors of some of the best papers from the Field Programmable Logic conference (FPL 03) and the Design and Test Europe conference (DATE’03). In all, seventy-nine authors, from research teams from all over the world, were invited to present their latest research in the extended format permitted by this special volume. The result is a valuable book that is a unique record of the state of the art in research into field programmable logic and reconfigurable computing. The contributions are organized into twenty-four chapters and are grouped into three main categories: architectures, tools and applications. Within these three broad areas the most strongly represented themes are coarse-grained architectures; dynamically reconfigurable and multi-context architectures; tools for coarse-grained and reconfigurable architectures; networking, security and encryption applications. Field programmable logic and reconfigurable computing are exciting research disciplines that span the traditional boundaries of electronic engineering and computer science. When the skills of both research communities are combined to address the challenges of a single research discipline they serve as a catalyst for innovative research. The work reported in the chapters of this book captures that spirit of that innovation.

Parallel Computing
Christian Bischof 2008

Reconfigurable Cryptographic Processor
Leibo Liu 2018-06-27 This book focuses on the design methods for reconfigurable computing processors for cryptographic algorithms. It covers the dynamic reconfiguration analysis of cryptographic algorithms, hardware architecture design, and compilation techniques for reconfigurable cryptographic processors, and also presents a case study of implementing the reconfigurable cryptographic processor, "Anole" designed by the authors' team. Moreover, it features discussions on countermeasures against physical attacks utilizing partially and dynamically reconfigurable array architecture to enhance security, as well as the latest trends for reconfigurable cryptographic processors. This book is intended for research scientists, graduate students, and engineers in electronic science and technology, cryptography, network and information security, as well as computer science and technology.

Energy Efficient Hardware-Software Co-Synthesis Using Reconfigurable Hardware
Jingzhao Ou
2009-10-14 Rapid energy estimation for energy efficient applications using field-programmable gate arrays (FPGAs) remains a challenging research topic. Energy dissipation and efficiency have prevented the widespread use of FPGA devices in embedded systems, where energy efficiency is a key performance metric. Helping overcome these challenges, Energy Efficient Hardware-Software Co-Synthesis Using Reconfigurable Hardware offers solutions for the development of energy efficient applications using FPGAs. The book integrates various high-level abstractions for describing hardware and software platforms into a single, consistent application development framework, enabling users to construct, simulate, and debug systems. Based on these high-level concepts, it proposes an energy performance modeling technique to capture the energy dissipation behavior of both the reconfigurable hardware platform and the target applications running on it. The authors also present a dynamic programming-based algorithm to optimize the energy performance of an application running on a reconfigurable hardware platform. They then discuss an instruction-level energy estimation technique and a domain-specific modeling technique to provide rapid and fairly accurate energy estimation for hardware-software co-designs using reconfigurable hardware. The text concludes with example designs and illustrative examples that show how the proposed co-synthesis techniques lead to a significant amount of energy reduction. This book explores the advantages of using reconfigurable hardware for application development and looks ahead to future research directions in the field. It outlines the range of aspects and steps that lead to an energy efficient hardware-software application synthesis using FPGAs.

Design of Low-Power Coarse-Grained Reconfigurable Architectures
Yoonjin Kim 2018-09-09 Coarse-grained reconfigurable architecture (CGRA) has emerged as a solution for flexible, application-specific optimization of embedded systems. Helping you understand the issues involved in designing and constructing embedded systems, Design of Low-Power Coarse-Grained Reconfigurable Architectures offers new frameworks for optimizing the architecture of components in embedded systems in order to decrease area and save power. Real application benchmarks and gate-level simulations substantiate these frameworks. The first half of the book explains how to reduce power in the configuration cache. The authors present a low-power reconfiguration technique based on reusable context pipelining that merges the concept of context reuse with context pipelining. They also propose dynamic context compression capable of supporting required hits of the context words set to enable and the redundant hits set to disable. In addition, they discuss dynamic context management for reducing power consumption in the configuration cache by controlling a read/write operation of the redundant context words. Focusing on the design of a cost-effective processing element array to reduce area and power consumption, the second half of the text presents a cost-effective array fabric that uniquely rearranges processing elements and their interconnection designs. The book also describes hierarchical reconfigurable computing arrays consisting of two reconfigurable computing blocks with two types of communication structures. The two computing blocks share critical resources, offering an efficient communication interface between them and reducing the overall area. The final chapter takes an integrated approach to optimization that draws on the design schemes presented in earlier chapters. Using a case study, the authors demonstrate the synergy effect of combining multiple design schemes.

Reconfigurable Computing: Architectures, Tools and Applications
Philip Brisk 2013-03-12 This book constitutes the thoroughly refereed conference proceedings of the 9th International Symposium on Reconfigurable Computing: Architectures, Tools and Applications, ARC 2013, held in Los Angeles, CA, USA, in March 2013. The 28 revised papers presented, consisting of 20 full papers and 11 poster papers were carefully selected from 41 submissions. The topics covered are applications, arithmetic, design optimization for FPGAs, architectures, place and routing.

The Computer Engineering Handbook
Vojin G. Oklobdzija 2001-12-26 There is arguably no field in greater need of a comprehensive handbook than computer engineering. The unparalleled rate of technological advancement, the explosion of computer applications, and the now-in-progress migration to a wireless world have made it difficult for engineers to keep up with all the developments in specialties outside their own. References published only a few years ago are now sorely out of date. The Computer Engineering Handbook changes all of that. Under the leadership of Vojin Oklobdzija and a stellar editorial board, some of the industry's foremost experts have joined forces to create what promises to be the definitive resource for computer design and engineering. Instead of focusing on basic, introductory material, it forms a comprehensive, state-of-the-art review of the field's most recent achievements, outstanding issues, and future directions. The world of computer engineering is vast and evolving so rapidly that what is cutting-edge today may be obsolete in a few months. While exploring the new developments, trends, and future directions of the field, The Computer Engineering Handbook captures what is fundamental and of lasting value.
heterogeneous-reconfigurable-processors-for-real-time-baseband-processing-from-algorithm-to-architecture

Digital Design and Fabrication - Vojin G. Oklobdzija 2017-12-19 In response to tremendous growth and new technologies in the semiconductor industry, this volume is organized into five, information-rich sections. Digital Design and Fabrication surveys the latest advances in computer architecture and design as well as the technologies used to manufacture and test them. Featuring contributions from leading experts, the book also includes a new section on memory and storage in addition to a new chapter on nonvolatile memory technologies. Developing advanced concepts, this sharply focused book—Describes new technologies that have become driving factors for the electronic industry Includes new information on semiconductor memory circuits, whose development best illustrates the phenomenal progress encountered by the fabrication and technology sector Contains a section dedicated to issues related to system power consumption Describes reliability and testability of computer systems Pinpoints trends and state-of-the-art advances in fabrication and CMOS technologies Describes performance evaluation measures, which are the bottom line from the user’s point of view Discusses design techniques used to create modern computer systems, including high-speed computer arithmetic and high-frequency design, timing and clocking, and PLL and DLL design

Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication - Shen, Jih-Shong 2010-06-30 Reconfigurable computing bring immense flexibility to on-chip processing while network-on-chip has improved flexibility in on-chip communication. Integrating these two areas of research reaps the benefits of both and represents the promising future of multiprocessor systems-on-chip. This book is the one of the first compilations written to demonstrate this future for network-on-chip design. Through dynamic and creative research into questions ranging from integrating reconfigurable computing techniques, to task assigning, scheduling and arrival, to designing an operating system to take advantage of the computing and communication flexibilities brought about by run-time reconfiguration and network-on-chip, it represents a complete source of the techniques and applications for reconfigurable network-on-chip necessary for understanding of future of this field.

Field Programmable Logic and Application - Jürgen Becker 2004-08-11 This book contains the papers presented at the 14th International Conference onFieldProgrammableLogicandApplications(FPL)heldduringAugust30th–September 1st 2004. The conference was hosted by the Interuniversity Micro-Electronics Center (IMEC) in Leuven, Belgium. The FPL series of conferences was founded in 1991 at Oxford University (UK), and has been held annually since: in Oxford (3 times), Vienna, Prague, Darmstadt, London, Tallinn, Glasgow, Villach, Belfast, Montpellier and Lisbon. It is the largest and oldest conference in reconfigurable computing and brings together academic researchers, industry experts, users and newcomers in an - formal, welcoming atmosphere that encourages productive exchange of ideas and knowledge between the delegates. The fast and exciting advances in field programmable logic are increasing steadily with more and more application potential and need. New ground has been broken in architectures, design techniques, (partial) run-time recon/igu-tion and applications of feld programmable devices in different areas. Many of these recent innovations are reported in this volume. The size of the FPL 2003 saw 216 papers submitted. The interest and support for FPL in the programmable logic community continued this year with 285 scientific papers submitted, demonstrating a 32% increase when compared to the year before. The technical program was assembled from 78 selected regular papers, 45 - editorial short papers and 29 posters, resulting in this volume of proceedings. The program also included three invited plenary keynote presentations from Xilinx,GliderTechnologyReportandAltera,anthreeembeddedtutorialfrom Xilinx, the Universit à at Karlsruhe (TH) and the University of Oslo.

Informatics in Control, Automation and Robotics - Dehuai Yang 2012-01-26 Session 2 includes 110 papers selected from 2011 3rd International Asia Conference on Informatics in Control, Automation and Robotics (CAR 2011), held on December 24-25, 2011, Shenzhen, China. As we all know, the ever growing technology in robotics and automation will help build a better human society. This session will provide a unique opportunity for the academic and industrial communities to address new challenges, share solutions, and discuss research directions for the future. Robotics research emphasizes intelligence and adaptability to cope with unstructured environments. Automation research emphasizes efficiency, productivity, quality, and reliability, focusing on systems that operate autonomously. The main focus of this session is on the autonomous acquisition of semantic information in intelligent robots and systems, as well as the use of semantic knowledge to guide further acquisition of information.

Multi-Processor System-on-Chip 1 - Liliana Andrade 2021-03-24 A Multi-Processor System-on-Chip (MPSoC) is the key component for complex applications. These applications put huge pressure on memory, communication devices and computing units. This book, presented in two volumes – Architectures and Applications – therefore celebrates the 20th anniversary of MPSoC, an interdisciplinary forum that focuses on multi-core and multi-processor hardware and software systems. It is this interdisciplinary which has led to MPSoC bringing together experts in these fields from around the world, over the last two decades. Multi-Processor System-on-Chip 1 covers the key components of MPSoCs: processors, memory, interconnect and interfaces. It describes advanced features of these components and technologies to build efficient MPSoC architectures. All the main components are detailed: use of memory and their technology, communication support and consistency, and specific processor architectures for general purposes or for dedicated applications.

Run-time Adaptation for Reconfigurable Embedded Processors - Lars Bauer 2010-12-01 Embedded processors are the heart of embedded systems. Reconfigurable embedded processors comprise an extended instruction set that is implemented using a reconfigurable fabric (similar to a field-programmable gate array, FPGA). This book presents novel concepts, strategies, and implementations to increase the run-time adaptivity of reconfigurable embedded processors. Concepts and techniques are presented in an accessible, yet rigorous context. A complex, realistic H.264 video encoder application with a high demand for adaptivity is presented and used as an example for motivation throughout the book. A novel, run-time system is demonstrated to exploit the potential for adaptivity and particular approaches/algorithm are presented to implement it.

Advanced Wireless Communications - Savo G. Gligic 2006-13 Fully revised and updated version of the successful "Advanced Wireless Communications" Wireless communications continue to attract the attention of both research community and industry. Since the first edition was published significant research and industry activities have brought the fourth generation (4G) of wireless communications systems closer to implementation and standardization. "Advanced Wireless Communications" continues to provide a comparative study of enabling technologies for 4G. This second edition has been revised and updated and now includes additional information on the components of common air interface, including the area of space time coding , multicarrier modulation especially OFDM, MIMO, cognitive radio and cooperative transmission. Ideal for students and engineers in research and development in the field of wireless communications, the second edition of Advanced Wireless Communications also gives an understanding to current approaches for engineers in telecom operators, government and regulatory institutions. New features include: Brand new chapter covering linear precoding in MIMO channels based on convex optimization theory. Material based on game theory modelling encompassing problems of adjacent cell interference, flexible spectra sharing and cooperation between the nodes in ad hoc networks. Presents and discusses the latest schemes for interference suppression in ultra wide band (UWB) cognitive systems. Discusses the cooperative transmission and more details on positioning.

Reconfigurable Computing: Architectures, Tools and Applications - Jürgen Becker 2009-03-07 This book constitutes the refereed proceedings of the 5th International Workshop on Applied Reconfigurable Computing, ARC 2009, held in Karlsruhe, Germany, in March 2009. The 21 revised full papers together with the 3 keynote lectures were carefully reviewed and selected from about 100 submissions. The papers are organized in topical sections on FPGA security and bitstream analysis, fault tolerant systems, architectures, place and route technologies, cryptography, and resource allocation and scheduling, as well as on applications.

Fine- and Coarse-Grain Reconfigurable Computing - Stamatis Vassiliadis 2007-10-12 Fine- and Coarse-Grain Reconfigurable Computing gives the basic concepts and building blocks for the design of Fine- (or FPGA) and coarse-Grain Reconfigurable Architectures. Recently-developed integrated architecture design and software-
supported design flow of FPGA and coarse-grain reconfigurable architecture are also described. Part I consists of two extensive surveys of FPGA and Coarse-Grain Reconfigurable Architectures: The FPGA technology is defined, which includes architecture, logic block, structure, interconnect, and existing fine-grain reconfigurable architectures emerged from both academia and industry. Additionally, the implementation techniques and CAD tools developed to facilitate the implementation of a system in reconfigurable hardware by the industry and academia are provided. In addition the features, the advantages and limitations of the coarse-grain reconfigurable systems, the specific issues that should be addressed during the design phase, as well as representing the coarse-grain reconfigurable systems are explained. In Part II, case studies, innovative research results about reconfigurable architectures and design frameworks from three projects AMDREL, MOLEN and ADRES&DREC, and a new classification according to microcoded architectural criteria are described. Fine- and Coarse-Grain Reconfigurable Computing is an essential reference for researchers and professionals and can be used as a textbook by undergraduate, graduate students and professors. Foreword by Yale Patt, Jim Smith and Mateo Valero

Reconfigurable Logic-Pierre-Emmanuel Gaillard2018-09-03 During the last three decades, reconfigurable logic has been growing steadily and can now be found in many different fields. Field programmable gate arrays (FPGAs) are one of the most famous architecture families of reconfigurable devices. FPGAs can be seen as arrays of logic units that can be reconfigured to realize any digital systems. Their high versatility has enabled designers to drastically reduce time to market, and made FPGAs suitable for prototyping or small production series in many branches of industrial products. In addition, and thanks to innovations at the architecture level, FPGAs are now conquering segments of mass markets such as mobile communications. Reconfigurable Logic: Architecture, Tools, and Applications offers a snapshot of the state of the art of reconfigurable logic systems. Covering a broad range of architectures, tools, and applications, this book, Explores classical FPGA architectures and their supporting tools Evaluates recent proposals related to FPGA architecture and including the use of network-on-chips (NoCs) Examines reconfigurable processors that merge concepts borrowed from the reconfigurable domain into processor design Exploits FPGAs for high-performance systems, efficient error correction codes, and high-bandwidth network routers with built-in security Expounds on emerging technologies to enhance FPGA architectures, improve routing structures, and create non-volatile configuration flip-flops Reconfigurable Logic: Architecture, Tools, and Applications reviews current trends in reconfigurable platforms, providing valuable insight into the future potential of reconfigurable systems.

Low Power Design Essentials-Jan Rabaey2009-04-21 This book contains all the topics of importance to the low power designer. It first lays the foundation and then goes on to detail the design process. The book also discusses such special topics as power management and modals design, ultra low power, and low power design methodology and flows. In addition, coverage includes projections of the future and case studies.

Compilation and Synthesis for Embedded Reconfigurable Systems-João Manuel Paiva Cardoso2013-05-16 This book presents techniques to tackle the design challenges raised by the increasing diversity and complexity of emerging, heterogeneous architectures for embedded systems. It describes an approach based on techniques from software engineering called aspect-oriented programming, which allow designers to control today’s sophisticated design concepts, rather than merely single application source code. Readers are introduced to the basic concepts of an aspect-oriented, domain specific language that enables control of a wide range of compilation and synthesis tools in the partitioning and mapping of an application to a heterogeneous (and possibly multithreaded) existing coarse-grain reconfigurable system and illustrates the benefits of the approach developed for applications from avionics and digital signal processing. Using the aspect-oriented programming techniques presented in this book, developers can reuse extensive sections of their designs, while preserving the original application source-code, thus promoting developer productivity as well as architecture and performance portability. Describes an aspect-oriented approach for the compilation and synthesis of applications targeting heterogeneous embedded computing architectures. Includes examples using an integrated tool chain for compilation and synthesis. Provides validation and evaluation for targeted reconfigurable heterogeneous architectures. Enables design portability, given changing target devices Allows developers to maintain a single application source code when targeting multiple architectures.

Low-Power Processors and Systems on Chips-Christian Piquet2018-10-03 The power consumption of microprocessors is one of the most important challenges of high-performance chips and portable devices. In chapters drawn from Piquet’s recently published Low-Power Electronics, this volume addresses the design of low-power microprocessors in deep submicron technologies. It provides a focused reference for specialists involved in systems-on-chips, from low-power microprocessors to DSP cores, reconfigurable processors, memories, ad-hoc networks, and embedded software. Low-Power Processors and Systems on Chips is organized into three broad sections for convenient access. The first section examines the design of digital signal processors for embedded applications and techniques for reducing dynamic and static power at the electrical and system levels. The second part describes several aspects of low-power systems on chips, including hardware and embedded software aspects, efficient data storage, networks-on-chips, and applications such as routing strategies in wireless RF sensing and actuating devices. The final section discusses embedded software issues, including details on compilers, retargetable compilers, and co-verification tools. Providing detailed examinations contributed by leading experts, Low-Power Processors and Systems on Chips supplies authoritative information on how to maintain high performance while lowering power consumption in modern processors and SoCs. It is a must-read for anyone designing modern computers or embedded systems.

Advances in Computer Systems Architecture-ACSAC (Asia-Pacific Computer Systems Architecture Conference)2004-09-14 This book constitutes the refereed proceedings of the 9th Asia-Pacific Computer Systems Architecture Conference, ACSAC 2004, held in Beijing, China in September 2004. The 45 revised full papers presented were carefully reviewed and selected from 154 submissions. The papers are organized in topical sections on cache and memory, reconfigurable and embedded architectures, processor architecture and design, power and energy management, compiler and operating systems issues, application-specific systems, interconnection networks, prediction techniques, parallel architectures and programming, microarchitecture design and evaluation, memory and I/O systems, and others.

Recent Advances in Wireless Communications and Networks-Jia-Chin Lin2011-08-23 This book focuses on the current hottest issues from the lower layers to the upper layers of wireless communication networks and provides critical issues. The book covers the state of the art in this area and presents an authoritative understanding of the information on these topics to make it easily accessible to readers of any level. This book also maintains the balance between current research results and their theoretical support. In this book, a variety of novel techniques in wireless communications and networks are investigated. The authors attempt to present these topics in detail. Insightful and reader-friendly descriptions are presented to nourish readers of any level, from practicing and knowledgeable communication engineers to beginning or professional researchers. All interested readers can easily find noteworthy materials in much greater detail than in previous publications and in the references cited in these chapters.

Adaptive Signal Processing in Wireless Communications-Mohamed Ilnkahla2017-12-19 Adaptive signal processing play a key role in modern wireless communication systems. The concept of adaptation is emphasized in the Adaptation in Wireless Communications Series through a unified framework across all layers of the wireless protocol stack ranging from the physical layer to the application layer, and from cellular systems to next-generation wireless networks. This specific volume, Adaptive Signal Processing in Wireless Communications is devoted to adaptation in the physical layer. It gives an in-depth survey of adaptive signal processing techniques used in current and future generations of wireless communication systems. Featuring the work of leading international experts, it covers adaptive channel modeling, identification and equalization, adaptive modulation and coding, adaptive multiple-input-multiple-output (MIMO) systems, and cooperative diversity. It also addresses other important aspects of adaptation in wireless communications such as hardware implementation, reconfigurable processing, and cognitive radio. A second volume in the series, Adaptation and Cross-layer Design in Wireless Networks is devoted to adaptation in the data link, network, and application layers.

Reconfigurable Computing-Scott Hauck2010-07-26 Reconfigurable Computing marks a revolutionary and hot topic that bridges the gap between the separate worlds of hardware and software design—the key feature of
reconfigurable computing is its groundbreaking ability to perform computations in hardware to increase performance while retaining the flexibility of a software solution. Reconfigurable computers serve as affordable, fast, and accurate tools for developing designs ranging from single-chip architectures to multi-chip and embedded systems. Scott Hauck and Andre DeHon have assembled a group of the key experts in the fields of both hardware and software computing to provide an introduction to the entire range of issues relating to reconfigurable computing. FPGAs (field programmable gate arrays) act as the “computing vehicles to implement this powerful technology. Readers will be guided into adopting a completely new way of handling existing design concerns and be able to make use of the vast opportunities possible with reconfigurable logic in this rapidly evolving field. Designed for both hardware and software programmers Views of reconfigurable programming beyond standard programming languages Broad set of case studies demonstrating how to use FPGAs in novel and efficient ways

Embedded Computer Systems: Architectures, Modeling, and Simulation-Koen Bertels 2009-07-21 This book constitutes the refereed proceedings of the 9th International Workshop on Architectures, Modeling, and Simulation, SAMOS 2009, held on Samos, Greece, on July 20-23, 2009. The 18 regular papers presented were carefully reviewed and selected from 52 submissions. The papers are organized in topical sections on architectures for multimedia, multi/many cores architectures, VLSI architectures design, architecture modeling and exploration tools. In addition there are 14 papers from three special sessions which were organized on topics of current interest: instruction-set customization, reconfigurable computing and processor architectures, and mastering cell BE and GPU execution platforms.

Applied Reconfigurable Computing. Architectures, Tools, and Applications-Fernando Rincón 2020-03-25 This book constitutes the proceedings of the 16th International Symposium on Applied Reconfigurable Computing, ARC 2020, held in Toledo, Spain, in April 2020. The 18 full papers and 11 poster presentations presented in this volume were carefully reviewed and selected from 40 submissions. The papers are organized in the following topical sections: design methods & tools; design space exploration & estimation techniques; high-level synthesis; architectures; applications.

Emerging Technologies in Data Mining and Information Security-Aboul Ella Hassanien 2021 This book features research papers presented at the International Conference on Emerging Technologies in Data Mining and Information Security (IEMIS 2020) held at the University of Engineering & Management, Kolkata, India, during July 2020. The book is organized in three volumes and includes high-quality research work by academicians and industrial experts in the field of computing and communication, including full-length papers, research-in-progress papers and case studies related to all the areas of data mining, machine learning, Internet of things (IoT) and information security.

Algorithm-Architecture Matching for Signal and Image Processing-Guy Gogniat 2010-10-20 Advances in signal and image processing together with increasing computing power are bringing mobile technology closer to applications in a variety of domains like automotive, health, telecommunication, multimedia, entertainment and many others. The development of these leading applications, involving a large diversity of algorithms (e.g. signal, image, video, 3D, communication, cryptography) is classically divided into three consecutive steps: a theoretical study of the algorithms, a study of the target architecture, and finally the implementation. Such a linear design flow is reaching its limits due to intense pressure on design cycle and strict performance constraints. The approach, called Algorithm-Architecture Matching, aims to leverage design flows with a simultaneous study of both algorithmic and architectural issues, taking into account multiple design constraints, as well as algorithm and architecture optimizations, that couldn’t be achieved otherwise if considered separately. Introducing new design methodologies is mandatory when facing the new emerging applications as for example advanced mobile communication or graphics using sub-micron manufacturing technologies or 3D-Integrated Circuits. This diversity forms a driving force for the future evolutions of embedded system designs methodologies. The main expectations from system designers’ point of view are related to methods, tools and architectures supporting application complexity and design cycle reduction. Advanced optimizations are essential to meet design constraints and to enable a wide acceptance of these new technologies. Algorithm-Architecture Matching for Signal and Image Processing presents a collection of selected contributions from both industry and academia, addressing different aspects of Algorithm-Architecture Matching approach ranging from sensors to architectures design. The scope of this book reflects the diversity of potential algorithms, including signal, communication, image, video, 3D, Graphics implemented onto various architectures from FPGA to multiprocessor systems. Several synthesis and resource management techniques leveraging design optimizations are also described and applied to numerous algorithms. Algorithm-Architecture Matching for Signal and Image Processing should be on each designer’s and EDA tool developer’s shelf, as well as on those with an interest in digital system design optimizations dealing with advanced algorithms.